ETH zürich

Provably Correct Memory Management

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11th EuroSys Doctoral Workshop (EuroDW'17), Belgrade

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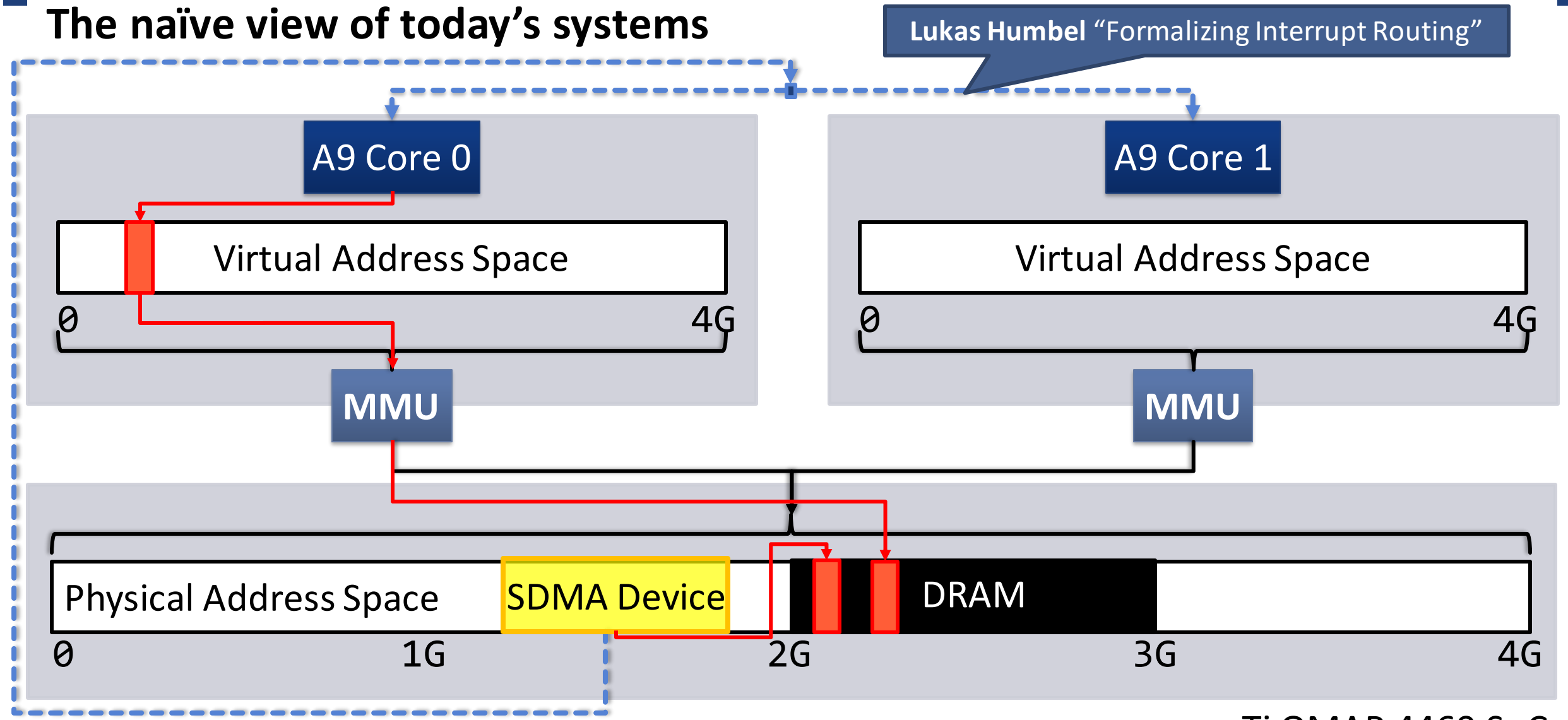
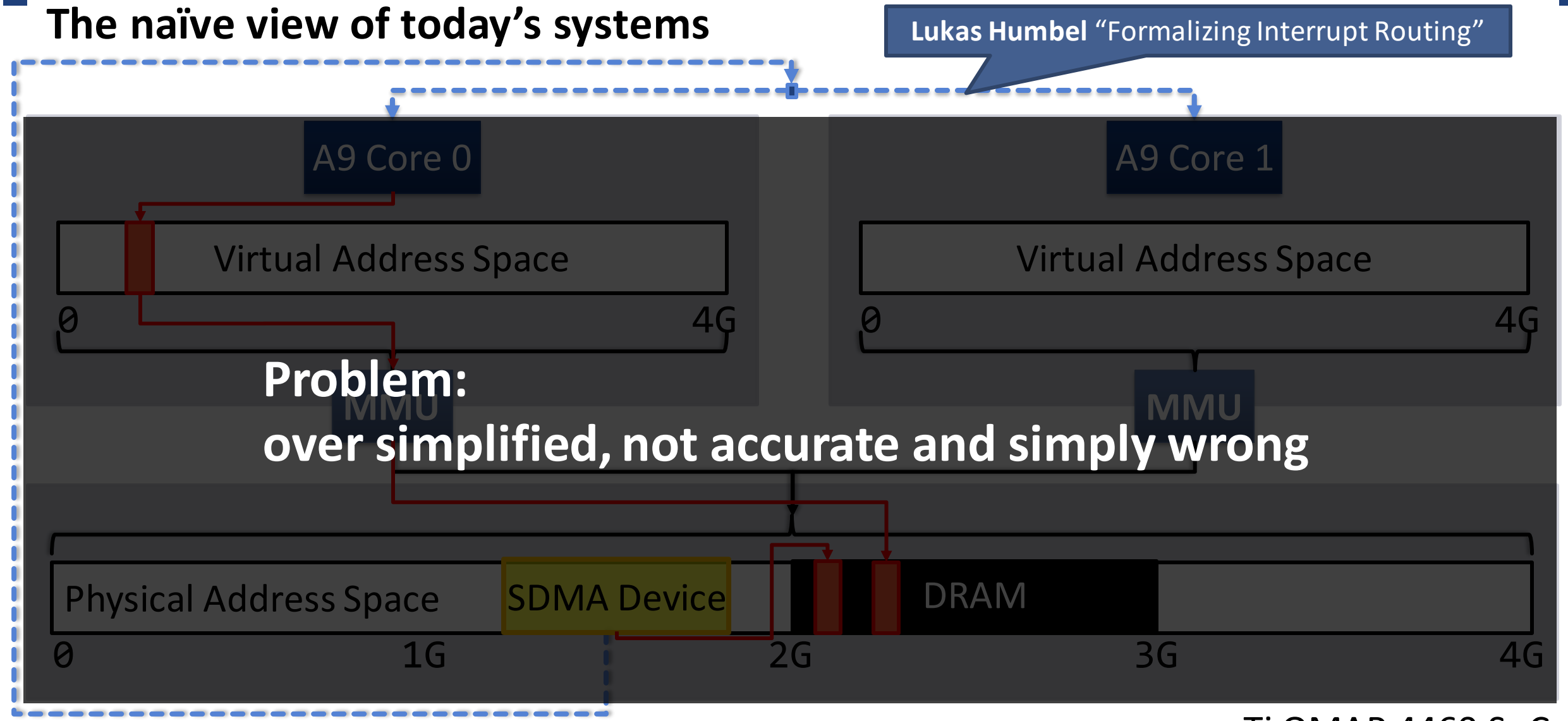
Systems@ETH zürich

The naïve view of today's systems



Ti OMAP 4460 SoC

The naïve view of today's systems

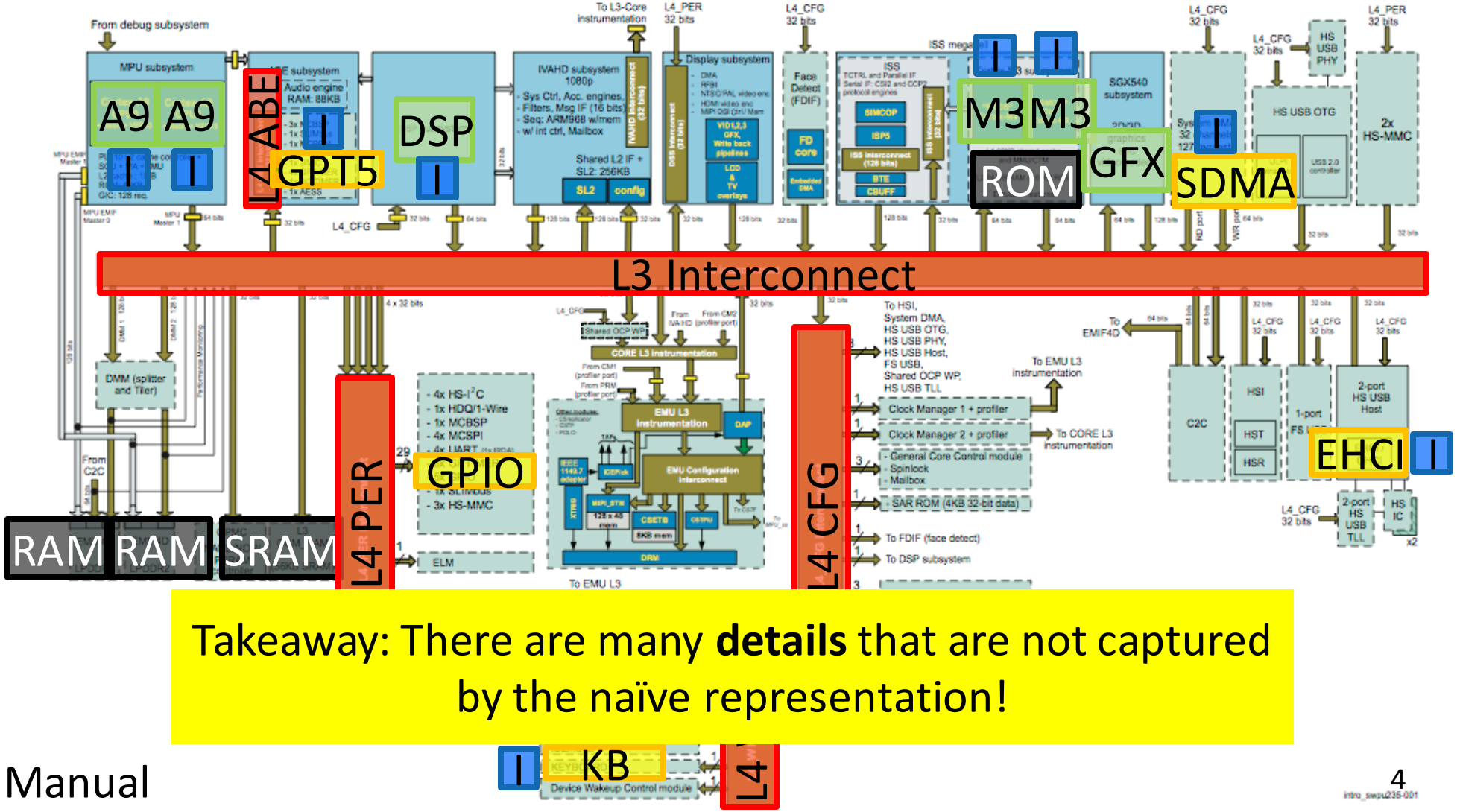


Ti OMAP 4460 SoC

Reality: The devil is in the details

Your mobile phone… 5-10 years ago!

- 6+ heterogeneous cores
- Private and shared memory
- 5+ Interconnects
- Devices attached to different interconnects
- Complex interrupt subsystem



Takeaway: There are many **details** that are not captured by the naïve representation!

OMAP 4460 SoC, Technical Reference Manual

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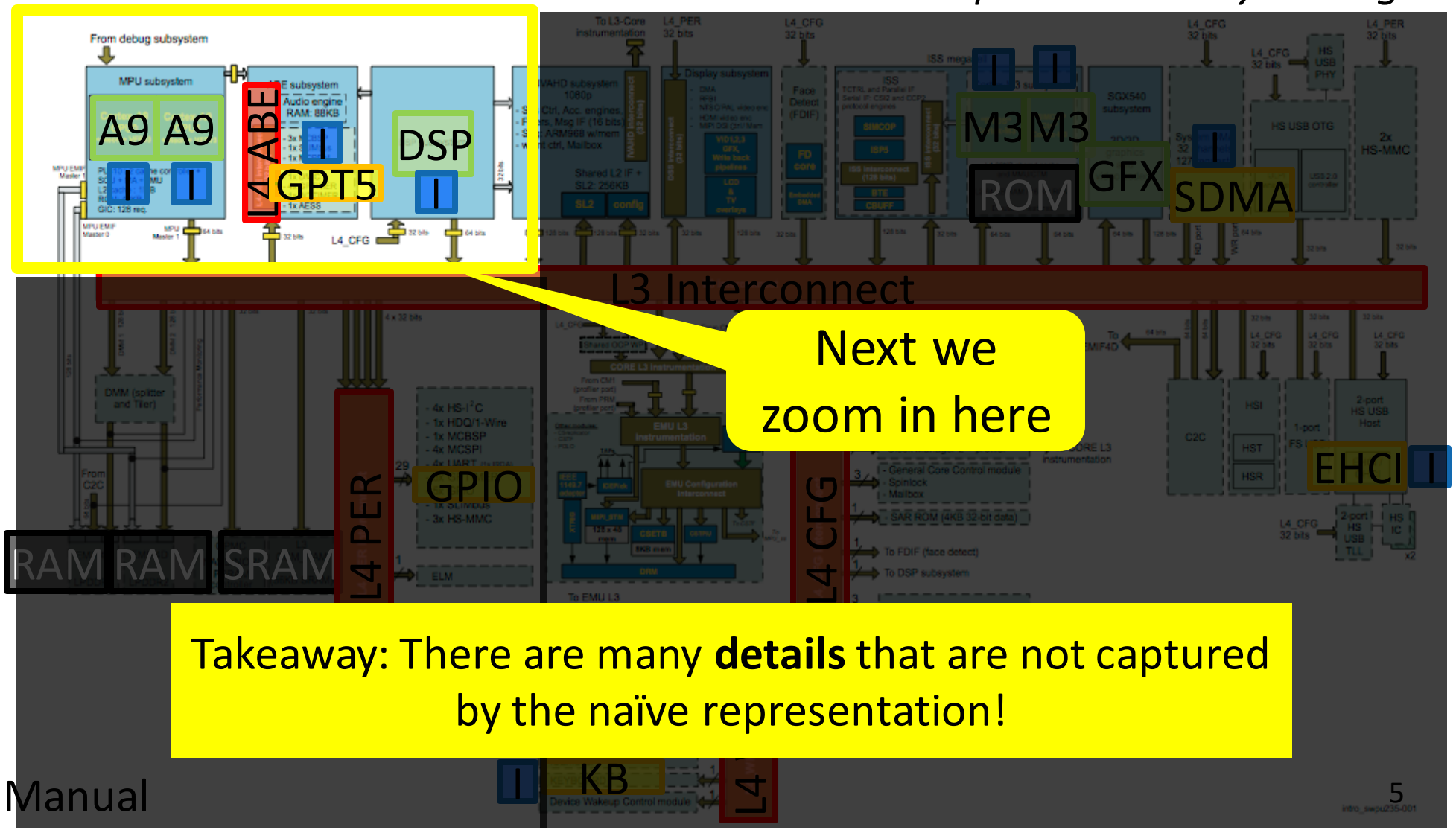
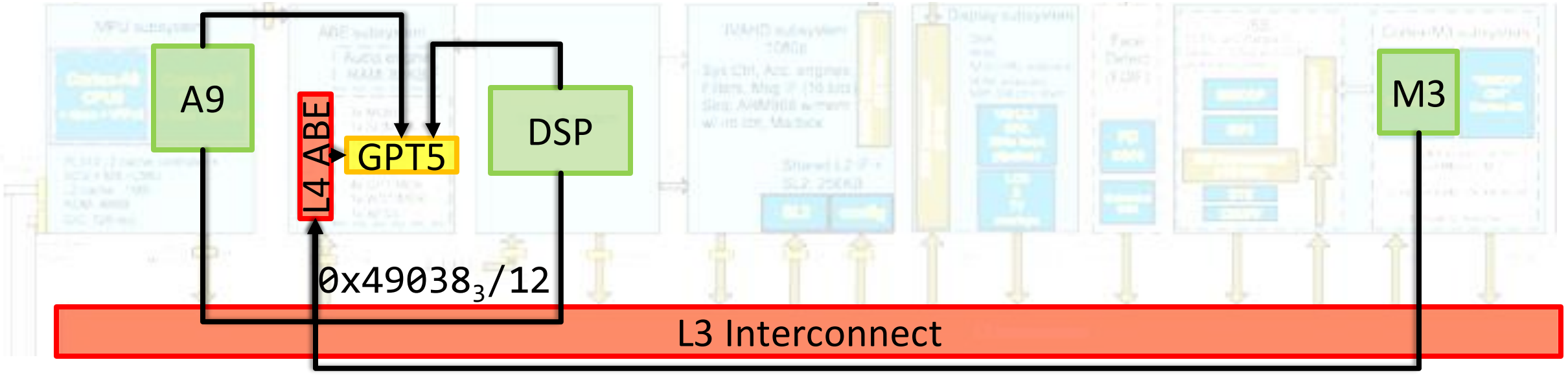


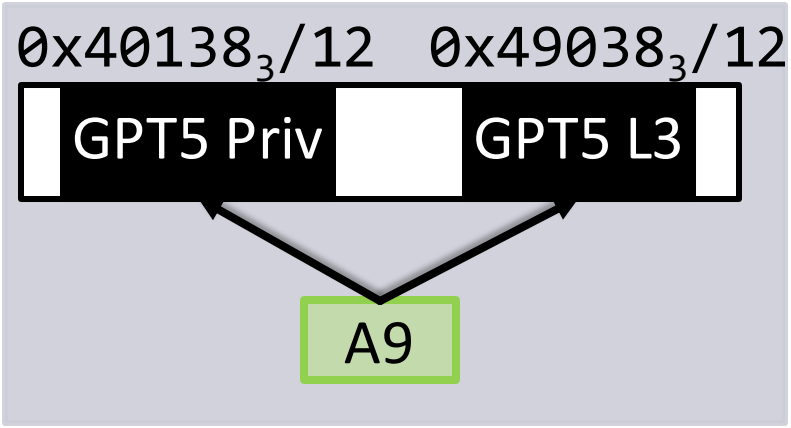
Takeaway: There are many **details** that are not captured by the naïve representation!

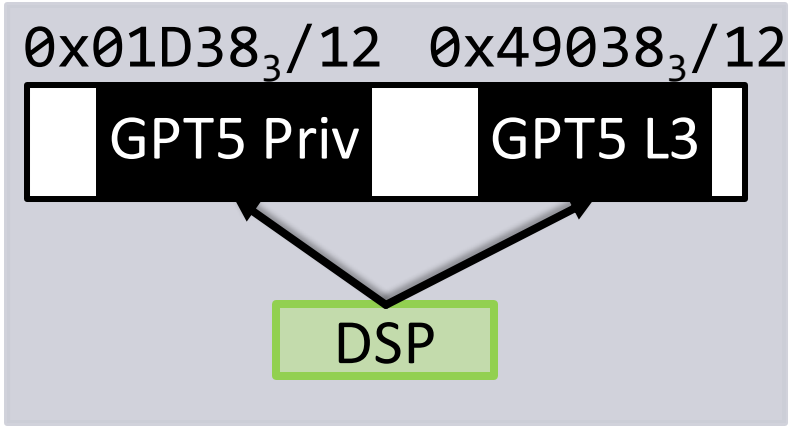
OMAP 4460 SoC, Technical Reference Manual

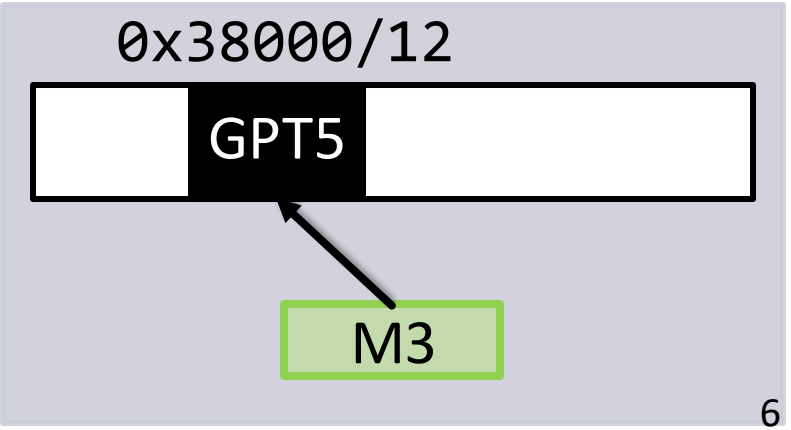
There is NO uniform view of the system

OMAP 4460 SoC









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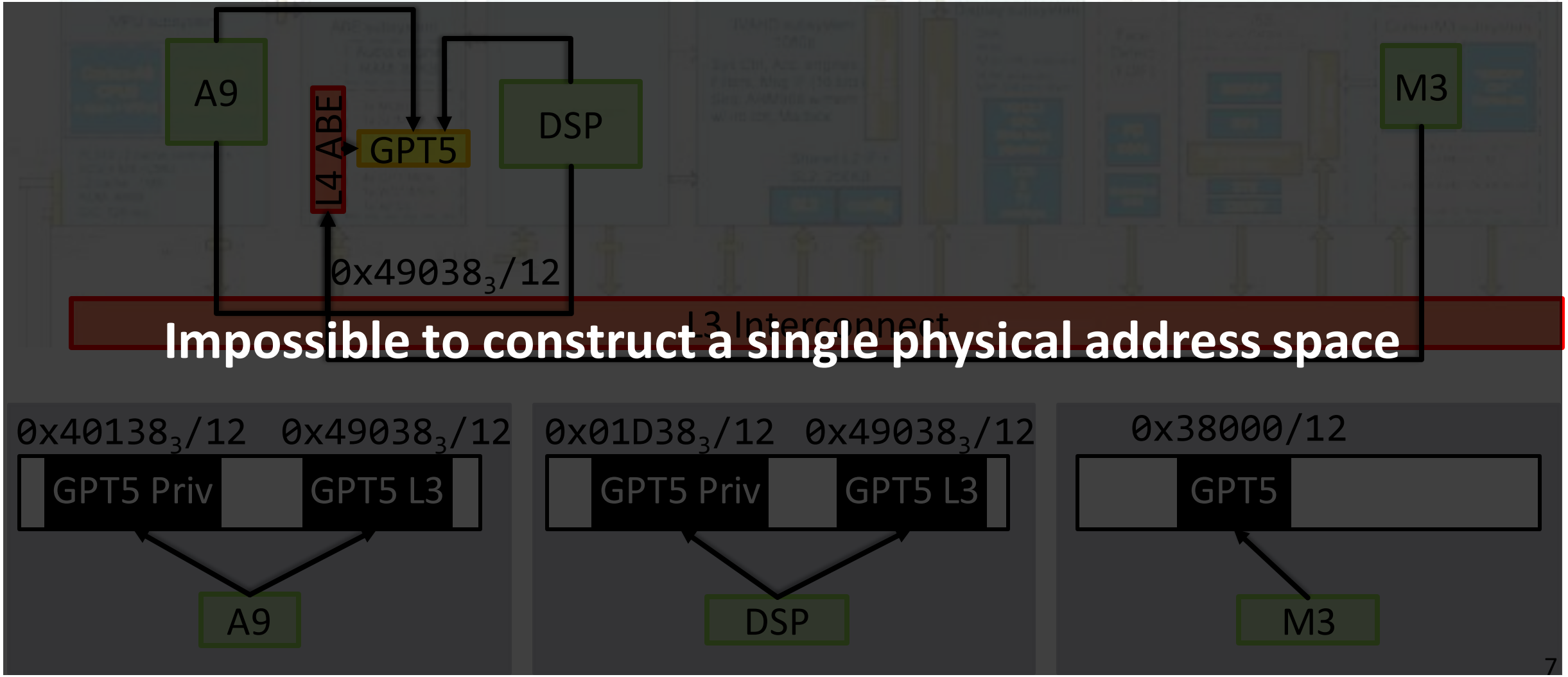
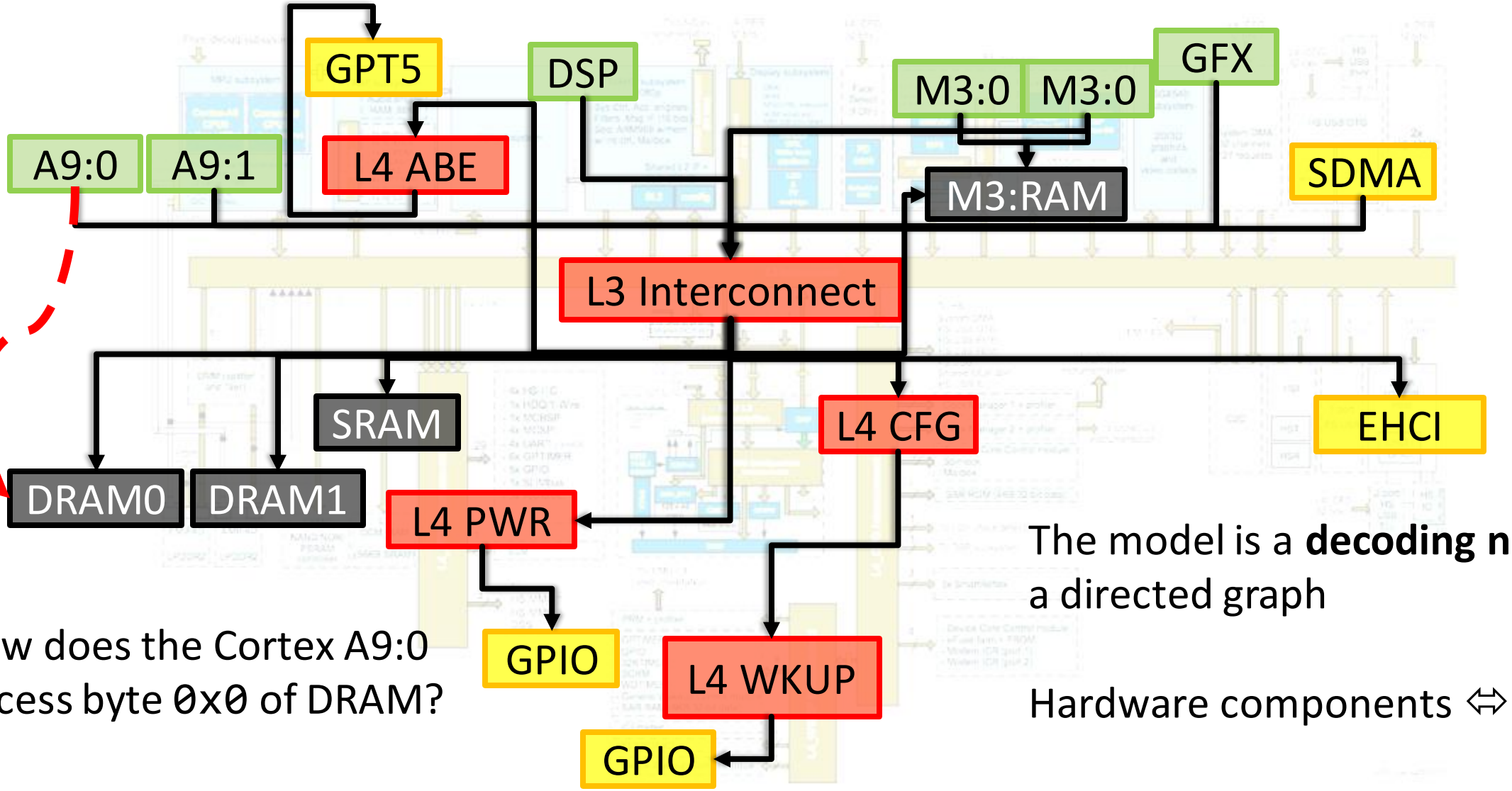
OMAP 4460 SoC



Why do we need a formal model for memory accesses ?

- We **build** systems and want to write **correct** systems code
- Experience from the Barrelfish operating system:
  dealing with this complexity every day.
  e.g. PCI programming, heterogeneity, resources, devices, new platforms
- Problem:
  - Current abstractions make the **wrong** assumptions
  - System software verification requires a sound system hardware description

A partial decoding net for the OMAP4460

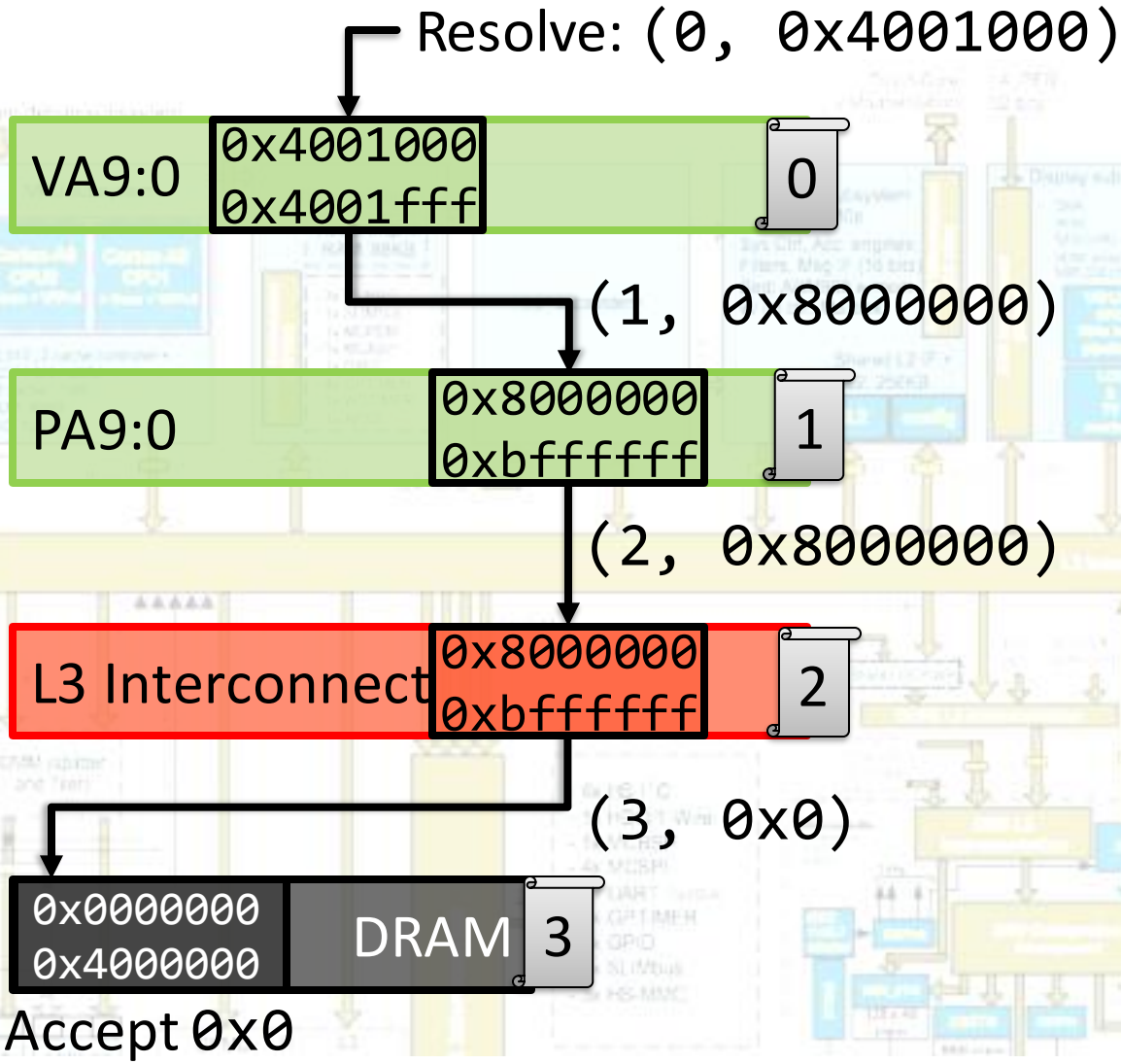


How does the Cortex A9:0
Access byte 0x0 of DRAM?

The model is a **decoding net,**
a directed graph

Hardware components ⇔ **nodes**

Modelling the access to byte 0x0 of DRAM from an A9 core



Each node has a label

Resolve a **name** (node, address)

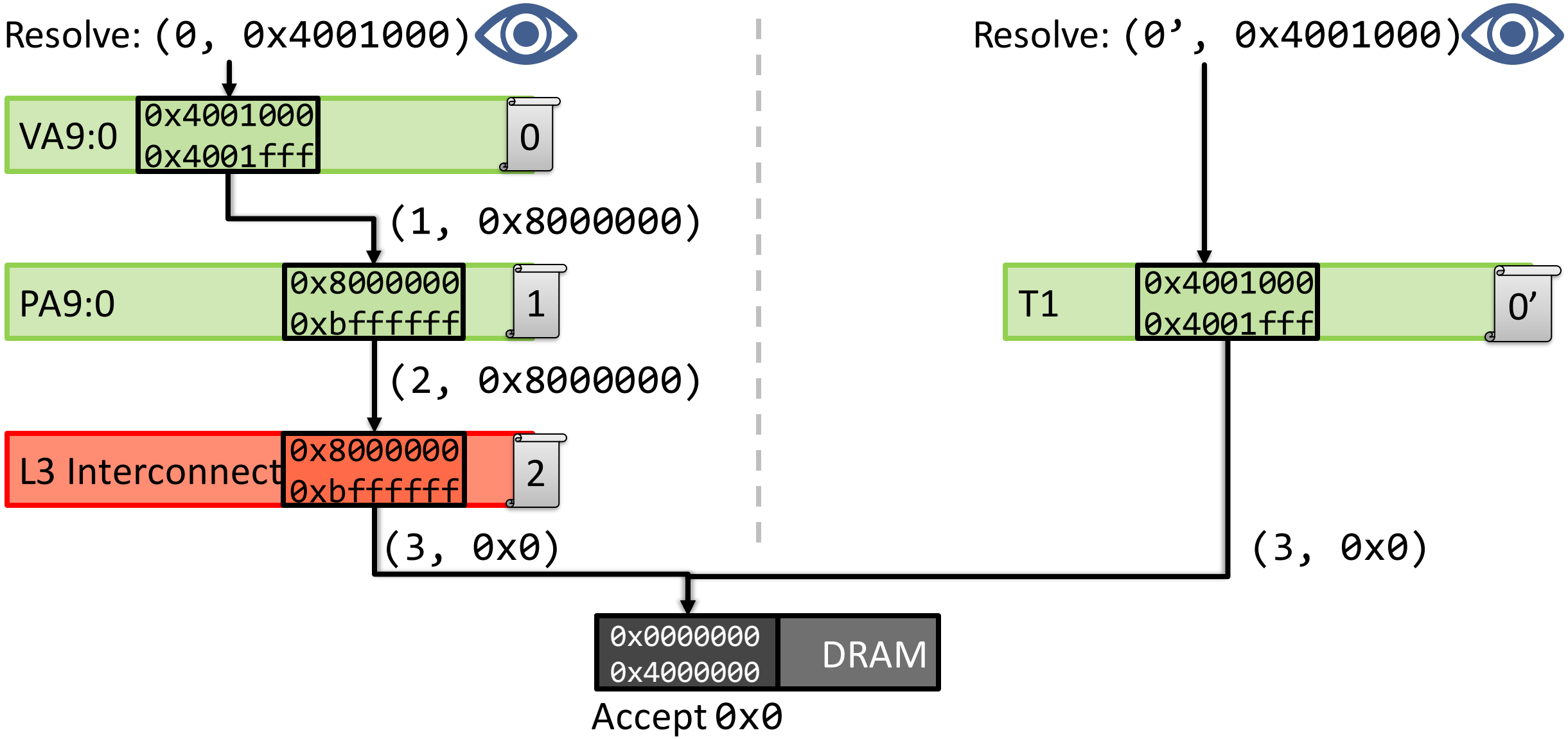
Model of one particular, static configuration state

Nodes have **two properties**:

$accept$: $node \rightarrow \{\mathbb{N}\}$

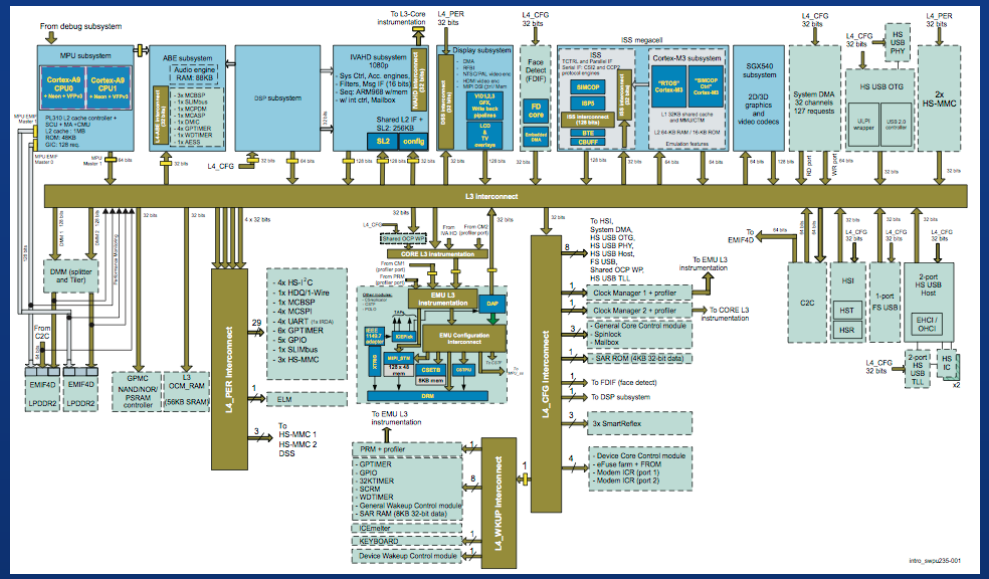
$translate$: $node \rightarrow \mathbb{N} \rightarrow \{name\}$

Flattening using view equivalence preserving operations



Flattening using view equivalence preserving operations

Resolve: (0, 0x4001000)



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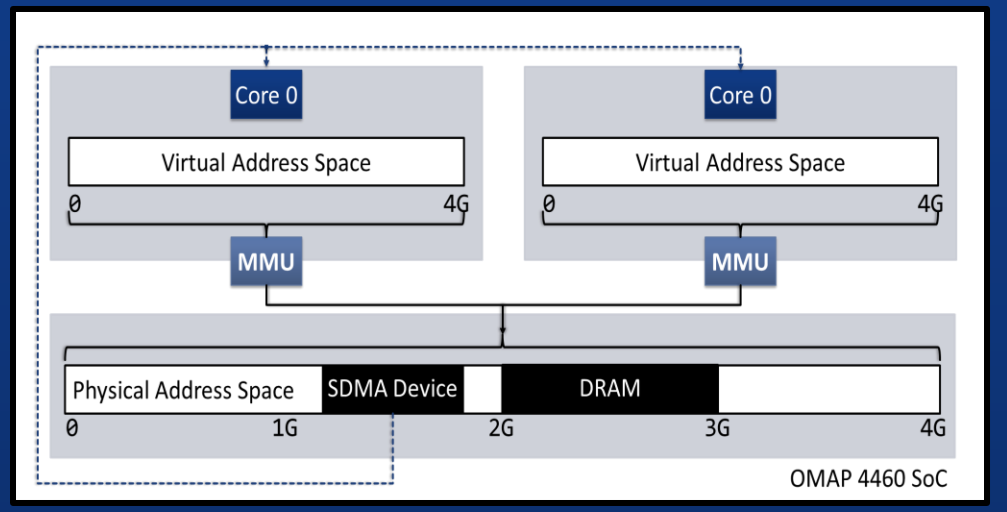
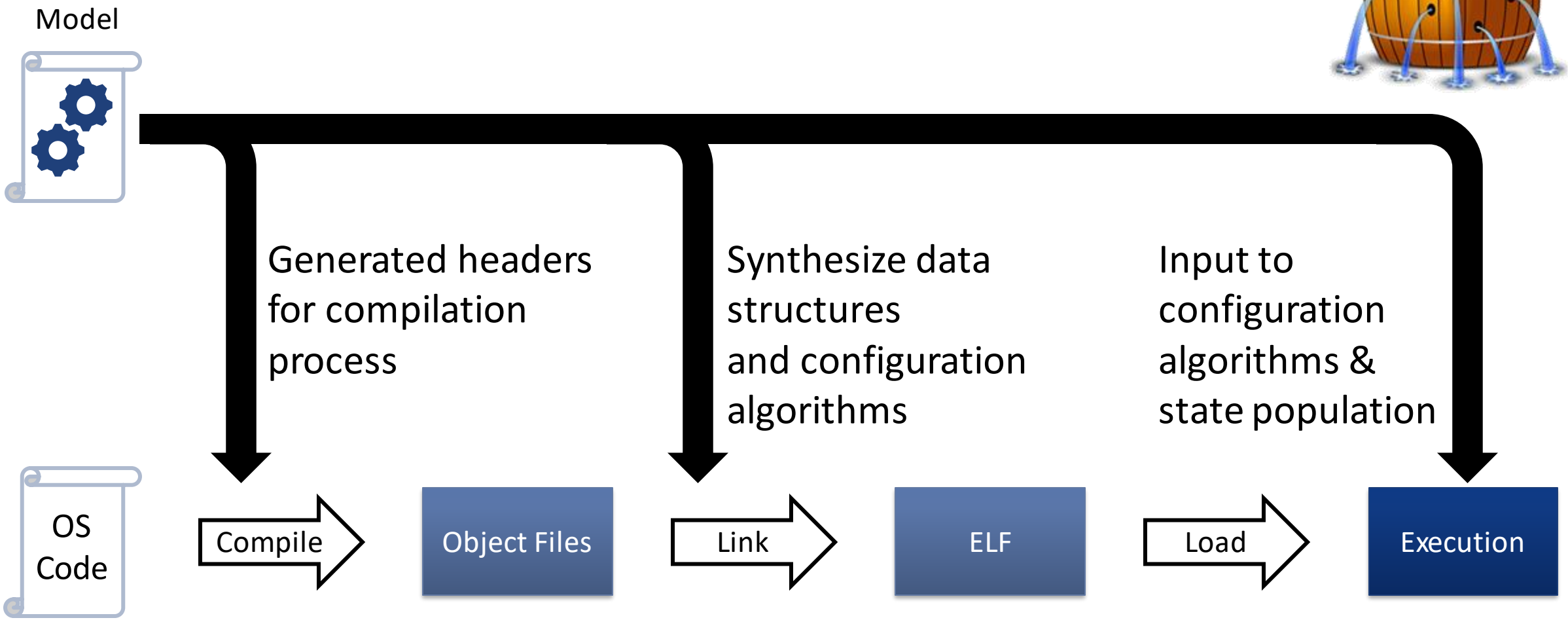


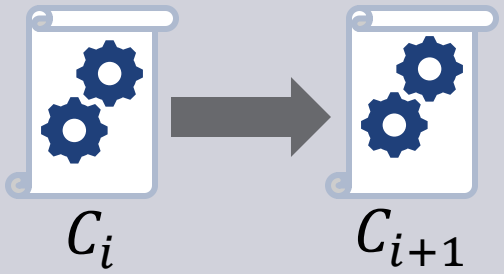
For ONE observer the flattened representation is equivalent to the textbook abstraction

Accept 0x0

Ongoing work: Using model output at compile and run time



Ongoing Work: Model applications



System (re-)configuration

- Generate system configuration from the model:
  - Kernel page tables
  - Initial capabilities
- **Synthesize** configuration algorithms
- **Transition** between configurations without violation of **invariants**
- **Constraints** on memory accesses

Future work: Model refinements

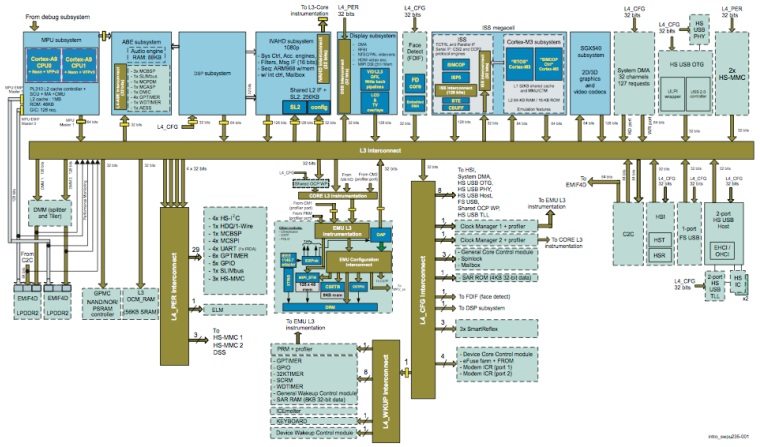
Distinction of Read/Write accesses

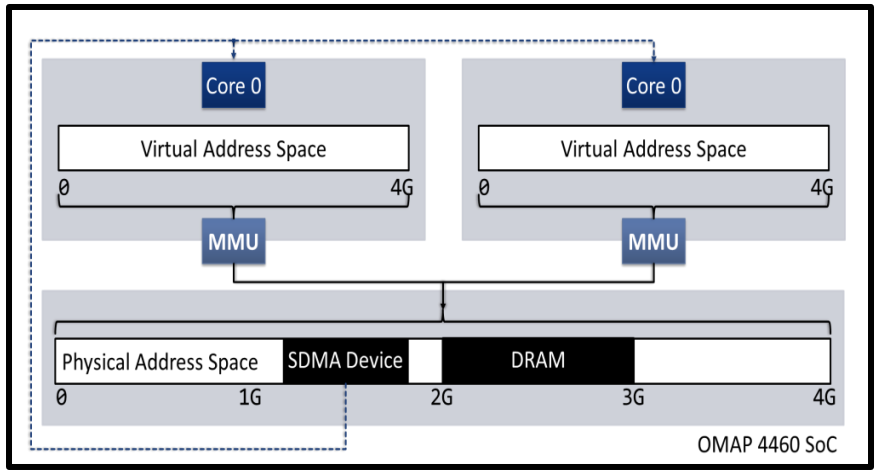
- Reads / writes have different semantics
- Write only / read only regions

Expressing performance characteristics

- Basis for a performance model.
- Resource allocation & scheduling

Summary





$V_{A9:0}$ **is map** $[20000_3/12$ **to** $P_{A9:0}$ **at** $80000_3]$

$P_{A9:0}, P_{A9:1}$ **are map** $[40138_3/12$ **to** GPT **at** $0]$ **over** $L3$

P_{DSP} **is map** $[1d3e_3/12$ **to** GPT **at** $0]$ **over** $L3$

V_{M3}, V_{M3} **are over** $L1_{M3}$

RAM_{M3} **is accept** $[55020_3/16]$

ROM_{M3} **is accept** $[55000_3/14]$

$V_{A9:1}$ **is map** $[20000_3/12$ **to** $P_{A9:1}$ **at** $80000_3]$

V_{DSP} **is over** P_{DSP}

$L2_{M3}$ **is map** $[0_{30}$ **to** $L3$ **at** $80000_3]$

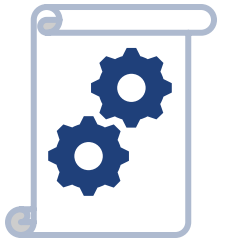
$L1_{M3}$ **is map** $[0_{28}$ **to** $MIF]$

$L4$ **is map** $[49038_3/12$ **to** GPT **at** $0]$

GPT **is accept** $[0/12]$

MIF **is map** $[0 - 5fffffff$ **to** $L2_{M3}, 55000_3/14$ **to** $RAM_{M3}, 55020_3/16$ **to** $ROM_{M3}]$

$L3$ **is map** $[49000_3/24$ **to** $L4$ **at** $40100_3, 55000_3/12$ **to** $MIF]$ **accept** $[80000_3/30]$



Configuration